REMARKS/ARGUMENTS

After entry of this amendment, claims 1-19 and 31-43 will remain pending in this application. Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Insenser Farre, United States patent number 6,460,172 (In) in view of Boerstler et al., United States patent number 5,668,507 (Bo). Claim 31 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over In in view of Bo in further view of Okazaki et al, United States patent number 6,282,503 (Ok). The other claims face similar rejections. Reconsideration of these rejections in light of these remarks is respectfully requested.

Drawings

The second sheet of the formal drawings, Figure 3, has been resent via express mail, label number EV 566 959 057 US.

Claim 1

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over In in view of Bo. But the combination of these references do not show or suggest each and every element of this claim. For example, claim 1 recites "providing the digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the emulation circuit." The cited references do not provide this feature either in separately or in combination.

The pending office action cites In, column 1, lines 35-36 and column 2, lines 30-39 as showing this limitation. (See pending office action, page 4, sixth paragraph.) These passages do not show providing a digital portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the emulation circuit as is required by the claim.

The first of the cited passages discusses conventional design tools used for designing various types of circuitry, specifically microprocessors, digital, and analog. The second passage states that it would be desirable to integrate these tools into one.

The claimed element requires a digital portion, the design of which is based on tests done on an analog portion while the emulation circuit configuration is modified. This is not taught by the existence or integration of design tools for different types of circuitry.

For at least this reason, claim 1 should be allowed.

Claim 31

Claim 31 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over In in view of Bo in further view of Ok. But these references do not teach each and every element of this claim. For example, claim 31 recites "providing said digital circuit portion, wherein said digital circuit portion may be formed by rewiring said emulation circuit. The cited references do not show or suggest this feature.

The pending office action cites the abstract, column 1, lines 33-35 and 43-49 as showing this feature. (See pending office action, page 24, second paragraph.) But these passages do not discuss rewiring an emulation circuit.

The abstract discusses a method of emulating a circuit using a number of small circuits and interconnect (presumably a programmable gate array, though this is not specified.) The first of the cited column 1 passages in Ok discusses emulating a logic circuit using component parts on a printed circuit board. The second passage discusses emulating an integrated circuit using conventional programmable gate arrays.

None of these passages discuss rewiring an emulation circuit to get a digital chip portion as is required by the claim. Rather, they discuss ways to emulate a circuit.

For at least this reason, claim 31 should be allowed.

Other claims

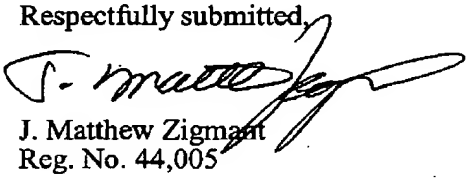
Claim 36 should be allowed for similar reasons as above. The other claims depend on the above claims, and should be allowed for at least the same reason and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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In re: application of: Vikram Gupta
Application Number: 09/618,971
Filed: July 19, 2000
Title: *Method for Designing Mixed Signal Integrated Circuits and Configurable Synchronous Digital Noise Emulator Circuit*
Atty Docket Number: **020408-000300US** JMZ/lo

Being faxed to **Examiner - Kandasamy Thangavelu** Group **2123** at facsimile number **1-703-872-9306** are the following documents:

1. This PTO/SB/97 Certificate of Transmission (1 page);
2. PTO/SB/30 Request for Continued Examination Transmittal Form (1 page submitted in duplicate);
3. PTO/SB/22 Petition for Extension of Time (1 page submitted in duplicate); and
4. Amendment (10 pages).

Number of pages being transmitted: 15

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